A wafer-handling robot upgrade results in

reduced wafer scratches

OVERVIEW Fabs operating cluster tools from the 1990s frequently report robot-related wafer scratching as a common source of yield loss. When scratching occurs, the probability of killing a die is nearly 100%. The dominant cause of wafer scratching in these tools is robot droop, a result of wear that causes the robot blade to use more of the vertical clearance between the wafers within a cassette. Faced with the probability of robot droop, a 200mm memory fab analyzed defect data to identify scratching in a set of tools. After evaluating options, the fab installed a robot upgrade that eliminated scratching and resulted in a payback on investment from higher yields within 10 weeks. Tool productivity also increased by 15% or more.

At the core of widely used manufacturing cluster tools are the wafer-handling robots, which, when introduced in the early 1990s, were considered state-of-the art. Over time, however, the OEM robot limitations have resulted in reduced tool productivity and yield. Among the potential problems are robot-induced particles generated by wafers sliding on the blade and exposed stainless steel bearings in the hub, elbow, and wrist assemblies. The slower operating speed of older robots also presents issues, as well as inaccurate placement of wafers due to sliding and imprecision in the robot arm joints. Tool downtime and parts costs often become concerns as robots age in volume manufacturing applications.

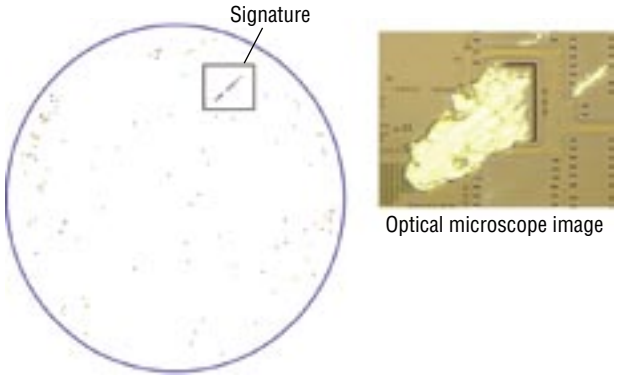

Figure 1. Wafer map of a production wafer (die layout removed) shows a robot-induced wafer scratch.

At the Samsung Austin Semiconductor fab, an effort was initiated to reduce scratch-related defects when a yield loss was identified on three PVD cluster tools. Many of Samsung's scratching incidents affected a random number of die and wafers within a production lot. Defect data was collected on several of these incidents, and tool-induced scratches were extracted from other yield-limiting events reported. This analysis identified a common signature that was highly repeatable in both its orientation and on-wafer location. **Figure 1** shows this scratch signature on a production wafer, along with an optical microscope image of the defect.

Dennis Winters, Samsung Austin Semiconductor LP, Austin, Texas
Richard Kent, Fabworx Solutions Inc., Newbury, New Hampshire

When in-line inspection and wafer electrical testing were performed, the source of scratches was narrowed to the PVD tools. Tool partitioning further revealed that scratches occurred while wafers were in the loadlock of the buffer chamber, and that the blade of the wafer-handling robot was the likely cause. To verify this, an experiment was conducted in which a cassette of bare wafers was loaded into the tool and the robot blade was extended into the cassette. Defect maps of those wafers revealed the same signature found on the production wafers, and blade-related scratching was confirmed.

Blade-related wafer scratches occur when the robot directly contacts the topside of a wafer while extended into the cassette, to either extract or return a wafer located in the above slot. The dominant cause of wafer scratching is robot droop, which occurs naturally as the robot ages and wears. As droop worsens, the robot blade uses more of the vertical clearance area between wafers within the cassette (**Fig. 2**). While much of this area is already used by the blade thickness, additional space is required when robot droop is considered. As blade-to-pitch clearance becomes smaller, wafer scratches become more likely.

Once robot droop was identified as the root cause of scratching, the PVD tool was taken out of production and maintenance was performed. Adjustments were made to level the robot blade and calibrate the cassette stage position. This resulted in a brief period during which wafer production resumed without scratching incidents. Over time, however, scratching returned. A consistent cycle then followed, where adjustments were made to the robot, production resumed, and scratching reoccurred. As the time between robot adjustments increased, scratching incidents became more frequent.

Determining a solution

Providing a more precise robot-to-cassette alignment became the first consideration, and a laser cassette aligner was evaluated. While this method was more accurate and objective, scratching consistently returned as robot droop increased. It then became clear that a more

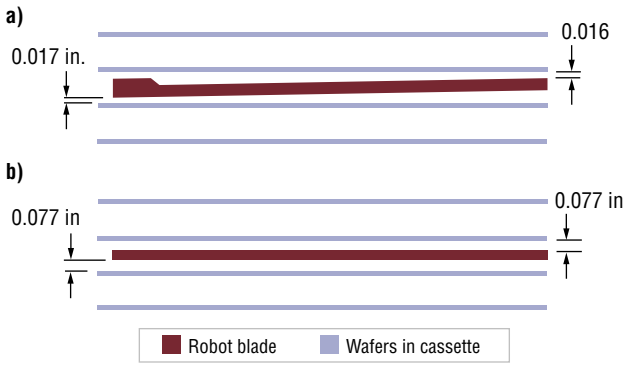

Figure 2. Comparison of robot droop: **a)** OEM robot droop after 8 months, and **b)** new robot droop after 13 months.

permanent solution was needed on the robot itself. Replacing only the robot's blade was not widely considered because the structural integrity of the entire arm contributes to droop. Upgrading the older-generation OEM robot with one that incorporated current technology and materials offered the potential to resolve scratching issues as well as other problems inherent to the OEM robot.

A robot upgrade was then installed in the buffer chamber on one of the three tools for evaluation. This robot, from Fabworx Solutions, incorporated several design enhancements that specifically address wafer scratching: tighter tolerances, precise adjustability, and a stronger, thinner blade to provide more blade-to-wafer clearance. Other performance issues [1] that were addressed included particles, placement repeatability, throughput, and maintenance costs.

Yield improvement results

Comparison of data collected both before and after the upgrade revealed a significant change in yield (**Fig. 3**). When scratching occurred prior to the upgrade, attributed yield loss was 0.4%. When a minimal impact average of 0.1% was assigned to this phenomenon for reporting purposes, a one-year return on investment of 513% resulted, with a payback interval of 10 weeks. No measurable droop was found in the new robot over a period of 11 months following the upgrade.

Increased productivity results

When a new process was implemented at Samsung Austin that utilized shorter process times, overall tool throughput became more dependent on (and limited by) the wafer handling systems. It was therefore estimated that increasing robot speed would provide greater overall tool throughput [2]. Since the upgraded robot's design reduced wafer sliding, robot speed could be safely increased. To further increase throughput, however, the transfer robot speed would also need to increase. A robot upgrade was therefore installed in the transfer chamber on the same tool, and an experiment was conducted to evaluate the productivity aspects of various robot speeds and process times. Random process times were studied using new (nonoptimized) slope (acceleration) settings on both robots. The resulting data (**Fig. 4**) indicated that increasing robot speed provided an overall tool throughput increase of 15% or more.

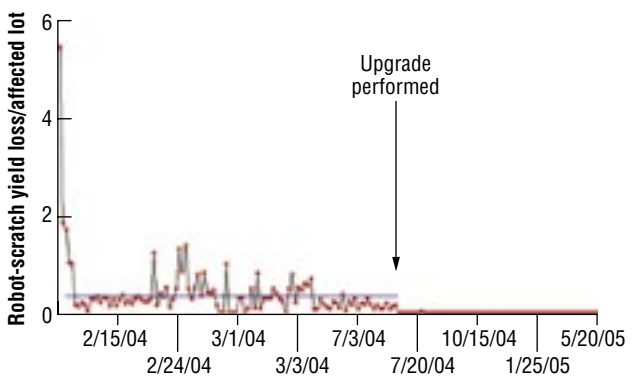

Figure 3. Robot-scratch yield loss per affected lot, before and after upgrade.

Decreased tool downtime, reduced parts usage

Prior to the upgrade, annual maintenance was required to replace the bearings and realign the robot. This procedure required 24 hr or more of tool downtime and an average bearing cost of $1500. The upgraded robot requires no annual bearing replacement, resulting in a savings in bearing cost, tool downtime, and technician labor. From a maintenance-only perspective, this resulted in a one-year return on investment of 65% with a payback interval of 1.5 years.

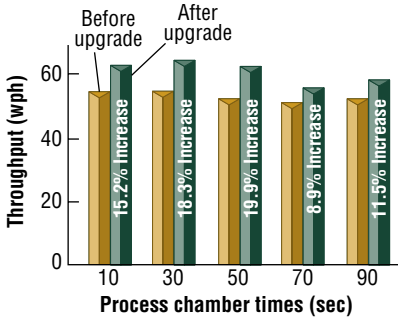

Figure 4. Throughput results show correlation between process time and increased throughput.

Conclusion

Although yield loss as a result of wafer scratching was the driving factor in the decision to upgrade these tools, other performance areas were also examined during this analysis. Improvements provided via the new robot were reviewed, and demonstrated considerable benefit. Robot droop was resolved, thus eliminating scratching. Tool productivity improved for various process steps, resulting in a throughput increase of 15% or more. Tool downtime and maintenance costs were reduced, accounting for an annual savings of $27,420 on these items alone. ■

Acknowledgments

Fabworx is a trademark of Fabworx Solutions Inc. The authors wish to acknowledge the following individuals for their assistance in the preparation of this article: Mike Dailey from Yarbrough Southwest; and Alan Stuber, Hunter Brugge, Ken Chinchilla, Matt Brackmann, Francisco de la Torre, Victor Coots, Wayne Rivers, Doni Parnell, John Paul Jose, Satori Matsumae, Vincent Burke, Quang Vuong, and the defect engineering department of Samsung Austin Semiconductor.

References

1. D. Angelo, S.-M. Suh, N. Khurana, K. Sankaranarayanan, "Improving Defect Performance through Better System Design," *Nanochip Technology Journal,* Issue Two, 2004.
2. K. Charles Janac, "The Expanding Role of Robots in Process Tool Productivity," *Solid State Technology,* Vol. 42, No. 1, p. 40, Jan. 1999.

continued on page 3

Reduced wafer scratches *continued from page 2*

Dennis Winters received his BS in chemistry from Emory U., Atlanta, GA, and is a senior process engineer at *Samsung Austin Semiconductor LP, 12100 Samsung Blvd., Austin, TX 78754; ph 512/672-1606, e-mail dwinters@sas.samsung.com.*

Richard Kent received his degree in engineering and is director of engineering for *Fabworx Solutions Inc., 122 Cheney Rd., Newbury, NH 03255; ph 603/938-5658, e-mail rkent@fabworx.com.*